REMARKS

Claims 1-19 remain pending in the present application. The Specification has been amended. Applicants have carefully and thoughtfully considered the Office Action and the comments therein. For the reasons given below, it is submitted that this application is in condition for allowance.

Amendments to the Specification

Applicants have amended the specification to correct several typographical errors.

Rejections under 35 USC § 102

On pages 2-5, in section 2, the Office Action, rejects claims 1, 8, and 17 under 35 U.S.C. § 102(b) as being anticipated by H. Jonathan Chao and Li-Shen Chen, *Delay-Bound Guarantee in Combined Input-Output Buffered Switches*, GLOBAL TELECOMMUNICATIONS CONFERENCE, 2000. GLOBECOM '00. IEEE, November 27, 2000 – December 1, 2000, Vol. 1, pgs. 515-524 (hereinafter Chao). Applicants respectfully traverse the rejection.

Claim 1 recites, "[a]n apparatus to switch packets, each packet comprising at least one cell, comprising: a plurality of input queues, each input queue storing cells to be switched; a plurality of output queues, each output queue storing switched cells; a switch fabric coupling said input queues to said output queues, said switch fabric having memory, said switch fabric storing cells moved from said input queues to said switch fabric, said switch fabric storing cells based on said output queues; and a controller coupled to said input queues and said switch fabric, said controller determining input priorities for cells moving from said input queues to said switch fabric and output priorities for cells moving from said switch fabric to said output queues."

Chao, however, teaches a fixed-length switch, where variable-length packets are segmented into fixed-length cells at input and reassembled at output. Chao, pg. 515, left column, and Figure 1. The switch described in Chao utilizes a Switch Hierarchical Link Sharing (SHLS) in which a

hierarchical link sharing (HLS) algorithm is used to provide delay bound for each session and distributes excess bandwidth fairly according to the hierarchy without a speedup requirement. *Id.* The HLS algorithm is implemented at different places within the switch. Chao, pg. 519, section V, right column.

The device described in Chao contains non-blocking switches with VOQs on the inputs. Chao, pg. 516, section III.A., right column. An exemplary design of a non-blocking switch is depicted in Figure 1 and the implementation of the SHLS scheme, as it applies to the non-blocking switch of Figure 1, is depicted in Figure 3. Chao, pg. 516, section III.A., right column, and pg. 519, section V., right column. **Figure 3 of Chao does not represent an exemplary switch architecture**. Instead Figure 3 depicts communication between the various elements of the switch depicted in Figure 1. The non-blocking switch of Figure 1 performs the SHLS scheme in four steps, which may operate in parallel at each input and output port. Chao, pg. 517, left column. In the first step, each input controller (IPC), which controls the input queues, performs a WFQ operation and selects a packet with the smallest finishing time. Chao, "Step 1: Selection and request," pg. 517 and "IPC operation:," pgs. 519 and 520. The IPC then sends a request to its corresponding output port. *Id.* In the second step, the output arbitration processor (OAP), which controls the output ports, performs a WF^2Q scheme by selecting an eligible packet from the IPC with the smallest virtual finishing time. Chao, "Step 2: Grant," pg. 517 and "OAP operation:," pg. 520. The OAP then sends a request to its corresponding input port. *Id.* In the third step, the input arbitration processor (IAP), which controls the input ports, performs a WF^2Q scheme by selecting an eligible packet from the OAP with the smallest virtual finishing time. Chao, "Step 3: Accept," pg. 517 and "IAP operation:," pg. 521. **The IAP then transmits the packet from the VOQ to its corresponding output buffer**. *Id.* In the fourth step, once a cell is transmitted across the switch, the cell is stored in the output buffer, which is controlled by the output controller (OPC), until the entire packet is reassembled. Chao, "Step 4: Transmit," pg. 517 and "OPC operation:," pg. 521. Once the entire packet is reassembled, the OPC schedules it to be transmitted out via the outgoing link. *Id.*

Chao does not teach the claimed invention for at least the following reason. In particular, Chao does not teach "**a controller** . . . **determining input priorities for cells moving from said**

input queues to said switch fabric and output priorities for cells moving from said input switch fabric to said output queues," as recited in claim 1. In rejecting claim 1, the Office Action aligns "a controller" with the IPC and the OPC of Chao. Chao, Fig. 3. As discussed above, a cell, which belongs to a packet, is selected for transmission based on the virtual finishing time of the packet to which the cell belongs. Chao, pg. 516, section III.A., right column, and pg. 517, left column. A cell is transmitted through the switch depicted in Figure 1 of Chao only after three steps are completed. First, based on the virtual finishing time of each individual packet, the IPC selects a packet from the input queue **and sends a request to a corresponding output port**. Chao, "Step 1: Selection and request," pg. 517 and "IPC operation:," pgs. 519 and 520. Second, the OAP selects an eligible packet from the IPC **and sends a request to its corresponding input port**. Chao, "Step 2: Grant," pg. 517 and "OAP operation:," pg. 520. Third, the IAP selects an eligible packet from the OAP with the smallest virtual finishing time. Chao, "Step 3: Accept," pg. 517 and "IAP operation:," pg. 521. **The IAP then transmits the packet, which is comprised of cells, from its VOQ to a corresponding output buffer**. *Id.* Thus Chao teaches determining a virtual finishing time for packets, wherein the virtual finishing time of the packet determines **when a cell is moved from the input straight thought the switch to the output buffer**. Chao, pgs. 517 and 519-521 and Figures 1 and 3. The virtual finishing time of Chao does not determine when a cell is moved from the input to a memory of the switch and does not determine when a cell is moved from a memory of the switch to the output buffer. In fact, Chao does not even discuss the memory of the switch, and the Office Action needed to assert that the switch of Chao inherently has memory. In contrast, the controller in claim 1 "**determine[s] input priorities for cells moving from said input queues to said switch fabric and output priorities for cells moving from said switch fabric to said output queues**." Hence, Chao fails to teach "a controller . . . determining input priorities for cells moving from said input queues to said switch fabric and output priorities for cells moving from said input switch fabric to said output queues" as recited in claim 1.

Dependent claims 2-7 are allowable, at least, for being dependent from an allowable claim.

Claim 8 receipts, "[a]n apparatus to switch packets, each packet comprising at least one cell, comprising: a plurality of input queues, each input queue storing cells to be switched a plurality of

output queues, each output queue storing switched cells; a switch fabric coupling said input queues to said output queues, said switch fabric having memory, said switch fabric storing cells moved from said input queues to said switch fabric, said switch fabric storing cells based on said output queues; a controller transferring highest priority cells in said switch fabric from said switch fabric to said output queues, transferring highest priority cells available for transfer in said input queues from said input queues to said switch fabric, prioritizing arriving cells in said input queues based on times of said arriving cells to depart, and updating cells in said input queues available for transfer to said switch fabric."

Chao does not teach the claimed invention for at least the following reason. In particular, Chao does not teach "a controller **transferring highest priority cells** in said switch fabric **from said switch fabric to said output queues**," and "**transferring highest priority cells** available for transfer in said input queues **from said input queues to said switch fabric**," as recited in claim 8. In rejecting claim 8, the Office Action does not clearly align the "highest priority cells," the "transferring . . . from said switch fabric to said output queues," and the "transferring . . . from said input queues to said switch fabric," with elements of Choa. To the best of the Applicant's understanding, the Office Action is attempting to align "highest priority cells," the "transferring . . . from said switch fabric to said output queues," and the "transferring . . . from said input queues to said switch fabric," with the role of the IPC and the OPC in Chao. As discussed above, a cell is transmitted through the switch depicted in Figure 1 of Chao only after three steps are completed. First, based on the virtual finishing time of each individual packet, the IPC selects a packet from the input queue **and sends a request to a corresponding output port**. Chao, "Step 1: Selection and request," pg. 517 and "IPC operation:," pgs. 519 and 520. Second, the OAP selects an eligible packet from the IPC **and sends a request to its corresponding input port**. Chao, "Step 2: Grant," pg. 517 and "OAP operation:," pg. 520. Third, the IAP selects an eligible packet from the OAP with the smallest virtual finishing time. Chao, "Step 3: Accept," pg. 517 and "IAP operation:," pg. 521. **The IAP then transmits the packet from its VOQ to a corresponding output buffer**. *Id.* Thus Chao teaches transferring a cell, whose priority is determined according to the virtual finishing time of the packet to which the cell belongs, **from the input buffer directly through the switch to**

the output buffer. Chao, pgs. 517 and 519-521. The virtual finishing time of Chao does not determine when the highest priority cells are transferred from the switch fabric to the output queues and does not determine when the highest priority cells are transferred from the input queues to the switch fabric. In fact, Chao does not even discuss the memory of the switch, and the Office Action needed to assert that the switch of Chao inherently has memory. In contrast, the controller of claim 8, "**transfer[s] highest priority cells** in said switch fabric **from said switch fabric to said output queues**," and "**transfer[s] highest priority cells** available for transfer in said input queues **from said input queues to said switch fabric**." Hence, Chao fails to teach "a controller transferring highest priority cells in said switch fabric from said switch fabric to said output queues," and "transferring highest priority cells available for transfer in said input queues from said input queues to said switch fabric," as recited in claim 8.

Dependent claims 9-16 are allowable, at least, for being dependent from an allowable claim.

Claim 17 recites, "[a] method to switch packets in a time slot, each packet comprising at least one cell, comprising: (a) selecting and transferring highest priority cells stored in memory of a switch fabric from said switch fabric to output queues; (b) updating flow-control information of said switch fabric; (c) selecting and transferring highest priority cells stored in input queues from said input queues to said memory of said switch fabric based on said flow-control information; and (d) updating said flow-control information of said switch fabric."

Independent claim 17 recites subject matter that is similar to that recited in claims 1 and 8 which are both allowable over Choa as discussed above. Therefore, claim 17 is allowable for the same reasons discussed above in connection with claim 17.

Dependent claims 18 and 19 are allowable, at least, for being dependent from an allowable claim.

Rejection under 35 U.S.C. § 103(a)

On pages 6-8, in section 4, of the Office Action, claims 4, 5, 7, and 10 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Chao in view of Shang-Tse Chuang et al., *Matching Output Queuing with a Combined Input/Output-Queued Switch*, IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, June 30, 1999, Vol. 17, pgs. 1030-1039 (hereinafter Chao). Claims 4, 5, 7 and 10 depend from claim 1 or 8 and, thus, are allowable as being dependent from an allowable claim.

On pages 8-10, in section 5, of the Office Action, claims 6, 11, 13, and 14 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Chao in view of Rojas-Cessa et al., *CLXB-1: Combined Input-One-cell-Crosspoint Buffered Switch,* 2001 IEEE WORKSHOP ON HIGH PERFORMANCE SWITCHING AND ROUTING, May 31, 2001, pg. 324-329 (hereinafter Rojas-Cessa). Claims 6, 11, 13, and 14 depend from claim 1 or 8 and, thus, are allowable as being dependent from an allowable claim.

On pages 10-11, in section 6, of the Office Action, claim 15 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Chao in view of Hui Zhang, *Service Disciplines for Guaranteed Performance Service in Packet-Switching Networks*, PROCEEDINGS OF THE IEEE, October 31, 1995, pgs. 1374-1396 (hereinafter Zhang). Claim 15 depends from claim 8 and, thus, is allowable as being dependent from an allowable claim.

On pages 11-12, in section 7, of the Office Action, claim 16 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Chao in view of Rojas-Cessa and further in view of Zhang. Claim 16 depends from claim 8 and, thus, is allowable as being dependent from an allowable claim.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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